Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A system clock divider comprising:

a divider register configured to store a mode indicator and a divisor indicator;

a divider configured to accept a first clock signal having a first frequency as an input and produce a second clock signal having a second frequency responsive thereto, said divider having a normal mode and a divide mode selectable via said mode indicator, wherein:

in said normal mode, said second frequency is substantially the same as said first frequency, and

in said divide mode, said second frequency is less said first frequency by a divisor value corresponding to said divisor indicator.

2. (Original) The system clock divider of claim 1, wherein said divisor value is selected from a set of divisor values including a first set of divisor values suitable for performance tuning, and a second set of divisor values suitable for power saving.

3. (Original) The system clock divider of claim 1, wherein said divisor value is selected from a set of divisor values, each of which equal are of the form 2^n, wherein n is a whole number.

4. (Original) The system clock divider of claim 1, wherein said set of divisor values is {2, 4, 8, 16, 32, 1024, 2048, 4096}.

5. (Original) A system clock divider comprising:

a divider register configured to store a mode indicator and a divisor indicator;

a divider configured to accept a first clock signal having a first frequency as an input and produce a second clock signal having a second frequency responsive thereto, said divider having a normal mode and at least two divide modes selectable via said mode indicator, wherein:

in said normal mode, said second frequency is substantially the same as said first frequency,

in said first divide mode, said second frequency is less said first frequency by a divisor value corresponding to said divisor indicator; and

in said second divide mode, said second frequency is less said first frequency by a divisor value corresponding to said divisor indicator, and wherein said second divide mode is entered and/or exited through the use of a user-countable millisecond interrupt signal.

6. (Original) The system clock divider of claim 5, wherein said divisor value is selected from a set of divisor values including a first set of divisor values suitable for performance tuning, and a second set of divisor values suitable for power saving.

7. (Original) The system clock divider of claim 5, wherein said divisor value is selected from a set of divisor values, each of which equal are of the form 2^n, wherein n is a whole number.

8. (Original) The system clock divider of claim 5, wherein said set of divisor values is {2, 4, 8, 16, 32, 1024, 2048, 4096}.

9. (Original) The system clock divider of claim 5, further including a medium mode.

10. (New) A system clock divider comprising:

a register configured to store a divisor indicator;

a divider configured to accept a first clock signal having a first frequency and produce a second clock signal having a second frequency, wherein in a normal mode, said second frequency is substantially the same as said first frequency, and in a divide mode, said second frequency is less said first frequency by an amount corresponding to said divisor indicator.